Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 91480

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2019

Third Semester

Electrical and Electronics Engineering

EE 6301 – DIGITAL LOGIC CIRCUITS

(Common to Electronics and Instrumentation Engineering, Instrumentation and Control Engineering)

(Regulations 2013)

(Also common to PTEE 6301 – Digital Logic Circuits for B.E.(Part-Time) – Third Semester – Electrical and Electronics Engineering – Regulations 2014)

Time : Three Hours | Maximum : 100 Marks

Answer ALL questions

PART – A **(10×2=20 Marks)**

1. Reduce $a(b+bc')+ab'$.
2. Convert 143_{10} into its binary and binary coded decimal equivalent.
3. Convert the given expression in canonical SOP form

   $Y = AC + AB + BC$.
4. Simplify the expression $Z = AB + A\bar{B}\cdot\left(\overline{\bar{A}.\bar{C}}\right)$.
5. Give the characteristic equation and characteristic table of SR flip-flop.
6. State any two differences between Moore and Mealy state machines.
7. What happens to the information stored in a memory location after it has been read and write operation ?

8. What is Programmable Logic Array ?

9. Write VHDL behavioral model for D flip-flop.

10. Write the VHDL code for a logical gate which gives high output only when both the inputs are high.

PART – B **(5×13=65 Marks)**

11. a) i) Convert 1010111011101100_2 into its octal, decimal and hexadecimal equivalent. **(6)**

ii) Deduce the odd parity hamming code for the data : 1010.

Introduce an error in the LSB of the hamming code and deduce the steps to detect the error. **(7)**

(OR)

b) i) With circuit schematic explain the operation of a two input TTL NAND gate. **(6)**

ii) With circuit schematic and explain the operation and characteristics of a ECL gate. **(7)**

12. a) Simplify the logical expression using K-map in SOP and POS form $F(A, B, C, D) = \Sigma m\ (0, 2, 3, 6, 7) + d(8, 10, 11, 15)$. **(13)**

(OR)

b) Design a full subtractor and realise using logic gates. Also, implement the same using half subtractors. **(13)**

13. a) i) Explain the operation of a master slave JK flip-flop. **(7)**

ii) Design a 3-bit bidirectional shift register. **(6)**

(OR)

b) i) Design a MOD-5 synchronous counter using JK flip-flops. **(7)**

ii) Design a sequence detector to detect the sequence 101 using JK flip-flop. **(6)**

14. a) Design an asynchronous sequential circuit that has two inputs X_2 and X_1 and one output Z. When $X_1 = 0$, the output Z is 0. The first change in X_2 that occurs while X_1 is 1 will cause output Z to be 1. The output Z will remain 1 until X_1 returns to 0.

(OR)

b) i) Implement the following function using PLA : **(7)**

$F(x, y, z) = \Sigma m(1, 2, 4, 6)$

ii) For the given Boolean function, obtain the hazard-free circuit. **(6)**

$F(A, B, C, D) = \Sigma m(1, 3, 6, 7, 13, 15)$.

15. a) Write a VHDL code to realize a full adder using behavioural modeling and structural modeling. **(13)**

(OR)

b) i) Discuss briefly the packages in VHDL. **(6)**

ii) Write an VHDL coding for realization of clocked SR flip-flop. **(7)**

PART – C **(1×15=15 Marks)**

16. a) i) A sequential circuit with D flip-flops A and B, input X and Y is specified by the following next state and output equations,

$A(t + 1) = AX + BX$,

$B(t + 1) = \overline{A}X$

$Y = (A + B)\overline{X}$

Draw the logic diagram, derive state table and state diagram. **(12)**

ii) Realize T flip-flop using JK flip-flop. **(3)**

(OR)

b) i) Design a full Adder using 4 × 1 multiplexer, also write its truth table and draw the logical diagram. **(10)**

ii) Describe level triggering and edge triggering. **(5)**
